



EUV LITHOGRAPHY ON THE MOVE FROM PRE- PRODUCTION TO PRODUCTION



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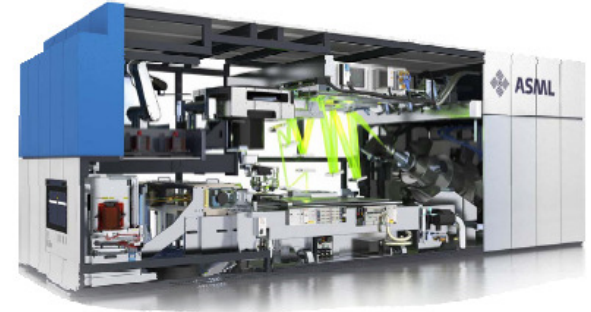
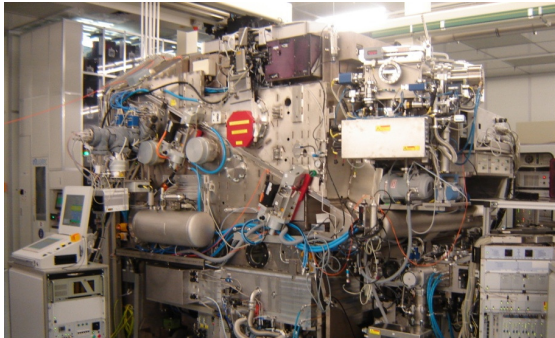
Introduction

NXE: 3100

NXE: 3300

Conclusions

IMEC EUV LITHOGRAPHY EXPOSURE TOOL ROADMAP



2006 - 2011	2011 - now	Installing now
ASML Alpha-Demo tool 40nm → 27nm LS 0.25 NA	ASML NXE:3100 – pre production 27nm, 22nm, 18nm LS 0.25 NA	ASML NXE:3300 – production 22, 16nm LS 0.33 NA

Improvements in Resists, masks, CD control, overlay, ...

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NXE:3100

Main specifications

- ▶ Field size: 26x33mm²
- ▶ NA=0.25 and $\sigma = 0.81$
- ▶ 6 off-axis illumination conditions available
- ▶ MMO vs NXT:1950i < 7nm

Track:TEL LITHIUS™ Pro for EUV
Discharge Produced Plasma source



SUSS MicroTec
MaskTrack Pro

EUV Technologies
Resist Outgassing tool



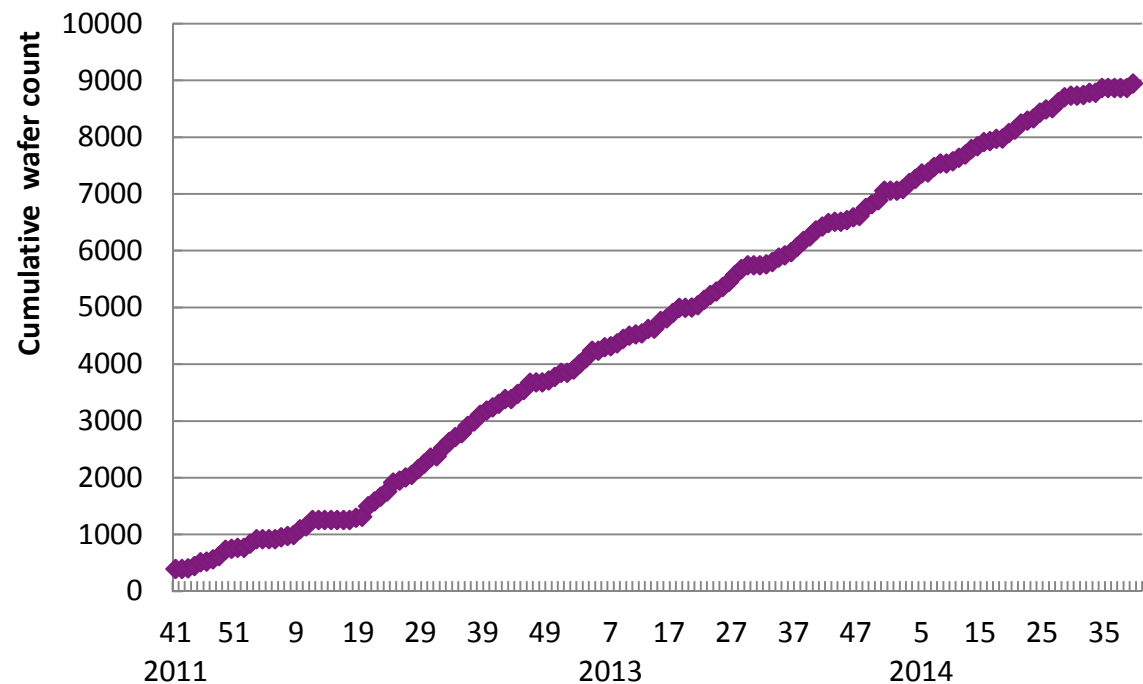
Session VII: Variability of EUV Resist Outgas Test Results

Ivan Pollentier

NXE:3100 PRODUCTIVITY

CUMULATIVE WAFERCOUNT

- ▶ 24/5 operation
- ▶ DPP source 2014 average power at IF 5.3W
- ▶ Average power at waferstage 390 microWatt/mm
- ▶ Average 2014 throughput 3-4 full wafers per hour
- ▶ Average system availability 2014 ~52%

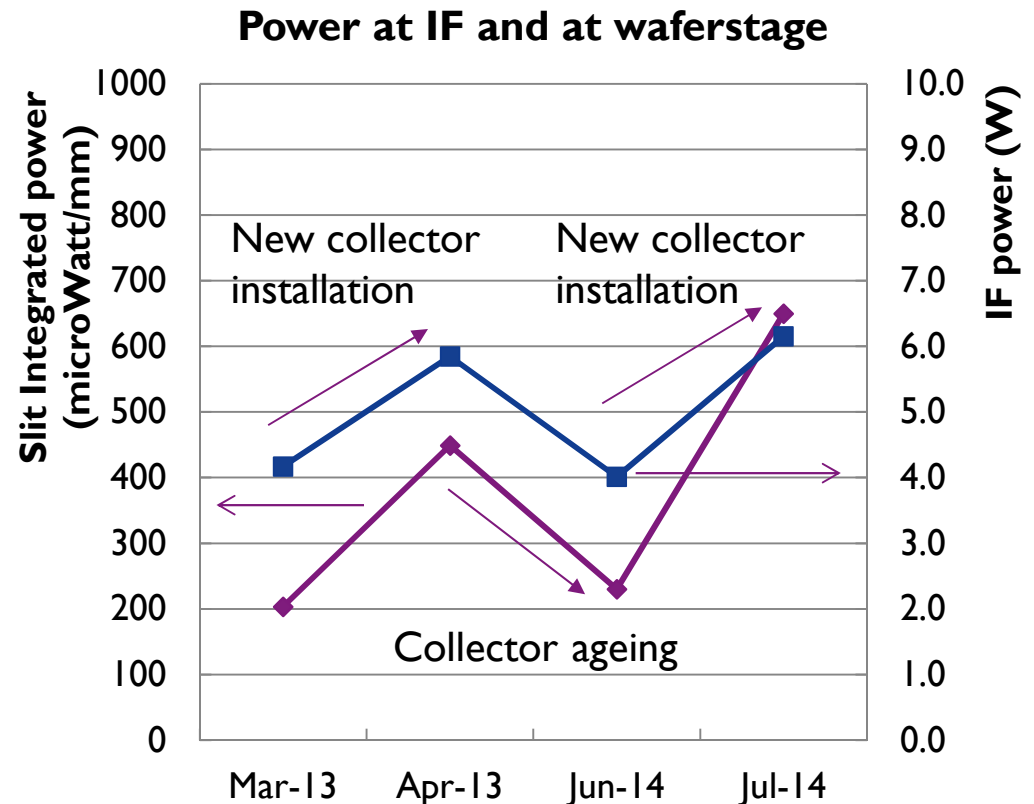


Cumulative wafercount of exposed wafers now exceeds 9000 wafers on NXE:3100

NXE:3100 PRODUCTIVITY

COLLECTOR LIFETIME AND IMPACT ON POWER

- ▶ In 2013-2014: NXE:3100 DPP source was operated using the same swap flange (collector mirror + debris mitigation) for ~9 months
- ▶ Due to low power on system, it was then decided to replace the swap flange (collector + debris mitigation system)
- ▶ Both power at IF and power at waferstage were fully recovered, improving productivity
- ▶ Post-mortem confirmed collector mirror erosion



After 3 years of operation, in July 2014 power was again at record high, with new source collector mirror (~9 months life)

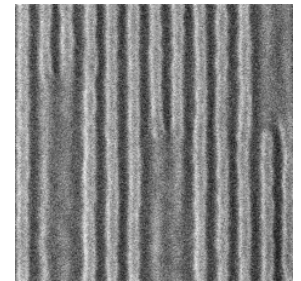
EUV MATERIALS

CAR ENABLEMENT AND ALTERNATIVE RESISTS

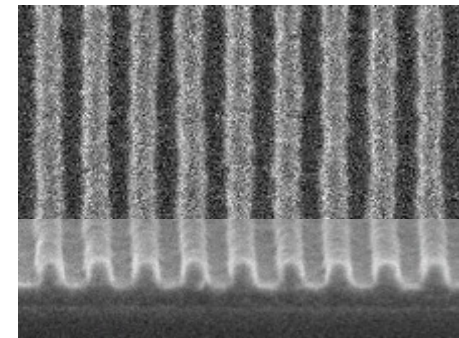
- ▶ None of the currently available CA EUV resists come close to the required $<4\text{nm}$ LWR at an acceptable sensitivity $<40\text{mJ}/\text{cm}^2$
- ▶ Optical resolution limit of NXE:3300 (26-30nm pitches) not yet printed in CA EUV resist

→ **Strong need for EUV resist post-treatment, or alternative EUV resists / materials**

- ▶ Investigating CAR enablement
 - Dry Development Rinse Process (Nissan Chemical)
 - Benefit demonstrated: collapse prevention
 - Challenge: LWR
 - Negative Tone Imaging (FFEM)
 - Currently comparable to positive tone imaging
 - Challenge: resolution



NTD imaging
HP 20nm – 0.25 NA
Dose 40 mJ/cm²



Initial data of CAR enablement promising
Final benefit to be demonstrated - FAB ready

FUJIFILM

EUV MATERIALS

CAR ENABLEMENT AND ALTERNATIVE RESISTS

- ▶ Metal containing resists – open to all collaborations

Early Exploratory Research
(Universities, Research Institutes,
New startup, resist vendors)

Not done at imec today

Synthesis
Simple Patterning (MET, PSI, EB)
Coupon Processing

Lab



imec
**Lab-to-Fab
Cross-Over**



imec
Fab

Advanced Patterning
Process Development
Integration in device flow

EUV scanner compliance (contamination, outgassing)

FAB\track compliance (contamination, compatibility with standard flows and chemicals)

Challenge:
Dose
85mJ/cm²

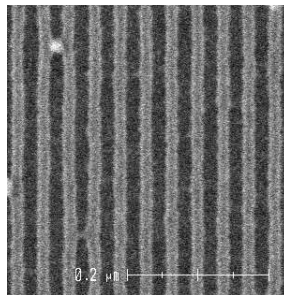
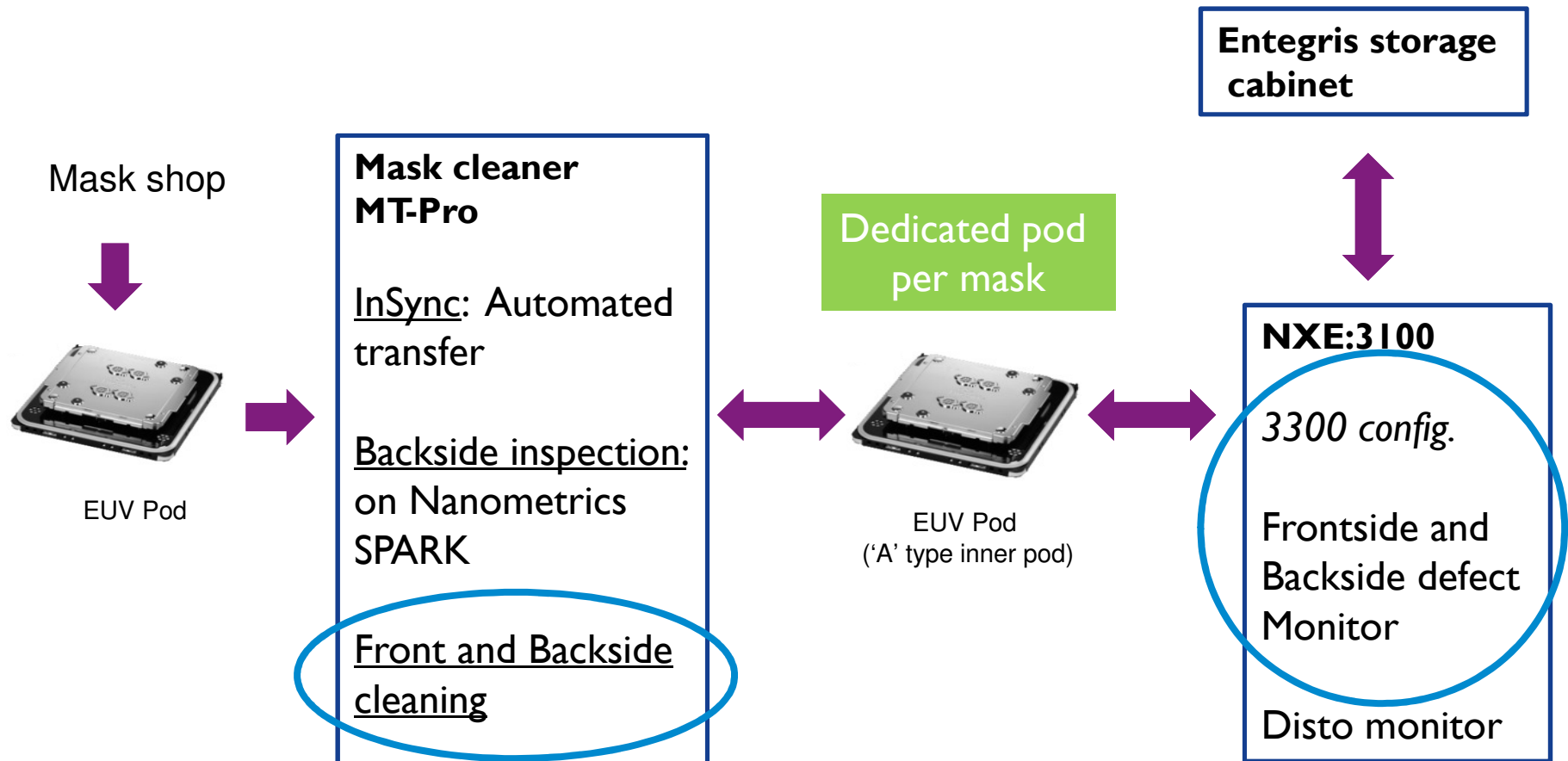


Photo condensable Metal Oxide resist (Inpria)
First 18nm LS pattern exposed on NXE:3100

Session IV: Progress on EUV Resist Materials and Processes at imec
Mieke Goethals

CAN WE KEEP THE EUV MASKS CLEAN?

MASK HANDLING IN PLACE AT IMEC

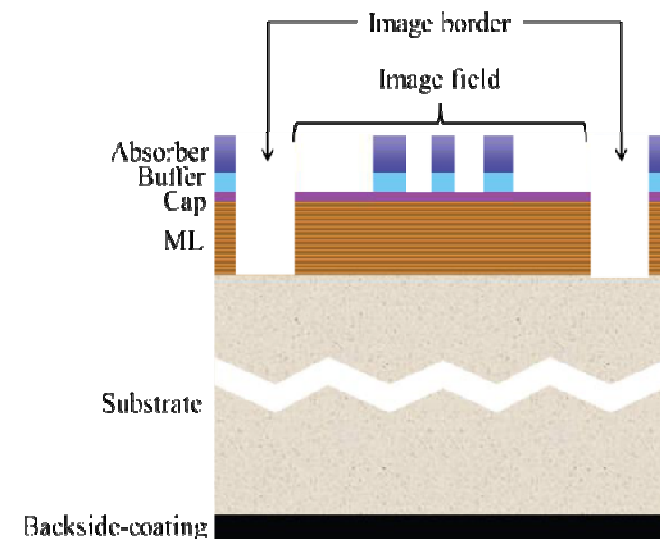
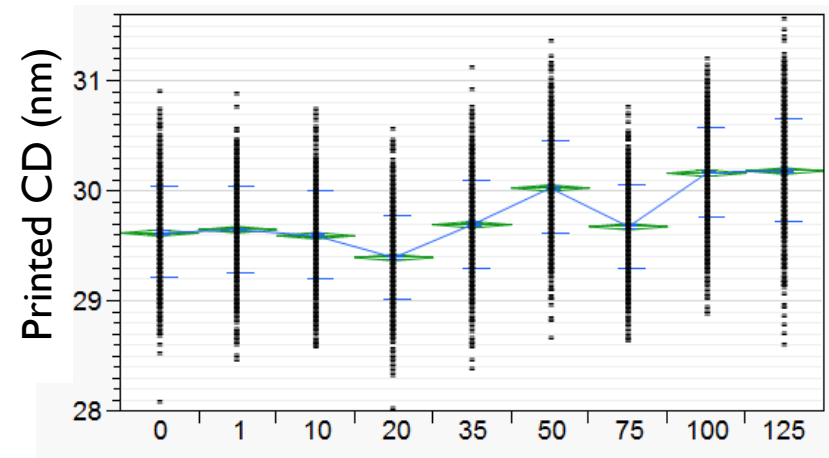


Infrastructure and procedures developed to limit and remove particle adders on mask frontside and backside

CAN WE KEEP THE EUV MASKS CLEAN?

LOW-IMPACT MASK CLEANING FLOW DEMONSTRATED

- ▶ Mask cleaning is required for
 - Small particles added to the frontside of the mask
 - Remove large particles from mask backside
- ▶ After optimizing mask cleaning recipe – demonstrated >100 cleans with no CD impact
- ▶ Mask cleaning evaluated on reticles with etched ML for dark image border generation
 - At field edge with etched ML – quantified cleaning impact as 5.6nm exposure field edge shift (4x) per clean (2 masks)

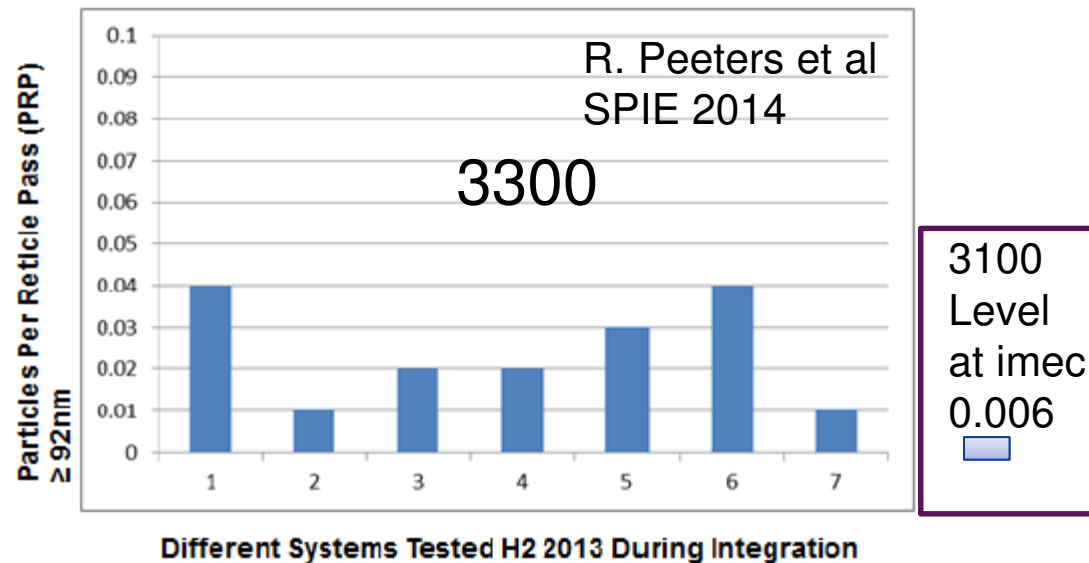


PMJ 2014: Towards reduced impact of EUV mask defectivity on wafer
Rik Jonckheere

CAN WE KEEP THE EUV MASKS CLEAN?

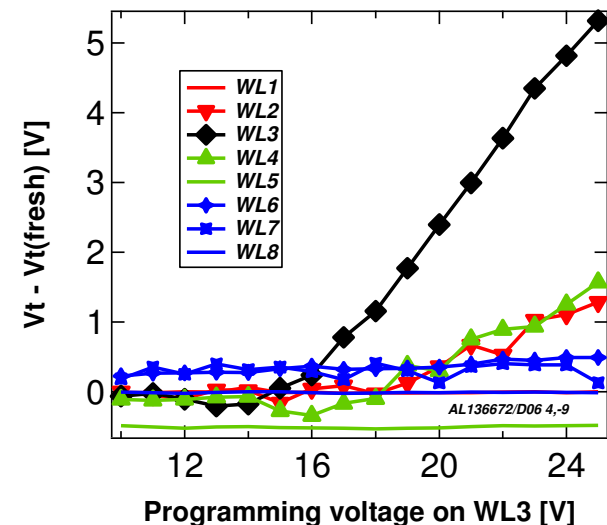
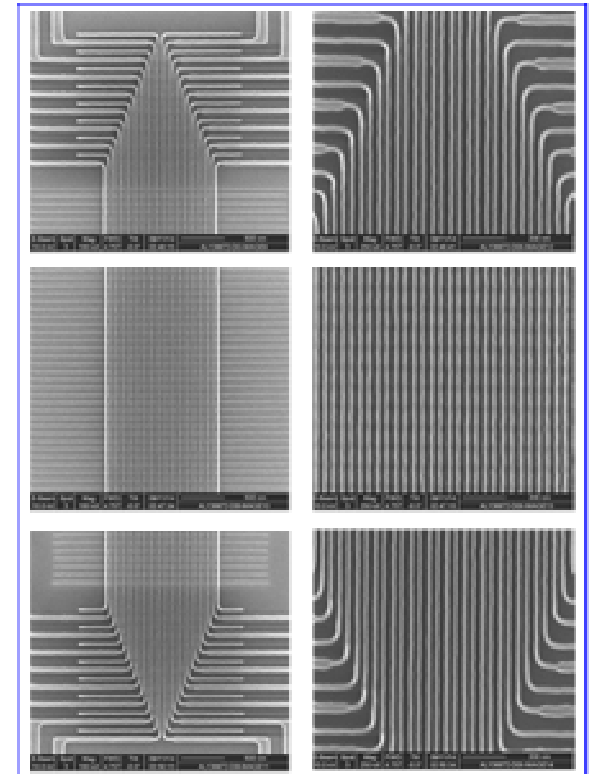
FRONTSIDE PARTICLE ADDERS IN 3100 SCANNER

- ▶ Methodology for estimating likelihood of frontside particle adder
 - Number of defects repeating from die-die on wafer, counts mask defects and particle adders on mask
 - Mask cycling in scanner was done, to increase mask handling
 - Increase of number of die-die repeating defects on wafer points to particle adder on mask
- ▶ By optimizing mask environment in 3100 scanner, a similar low chance for adding a particle is now demonstrated on 3100 as reported on 3300



ELECTRICALLY FUNCTIONAL FLASH CELL DEMONSTRATOR

- ▶ FLASH – 20nm Half Pitch (HP)
 - CG CORE: 80nm pitch EUV + Self Aligned Double Patterning (Spacer) patterning
 - Realizing 40nm pitch
 - Electrically working 8-cell strings demonstrated
- ▶ Proposed outlook: FLASH 15nm HP
 - Next step: 60nm pitch EUV – 15nm after SADP



*J. Versluijs, H. Hody, E. Vecchio, V. Paraschiv,
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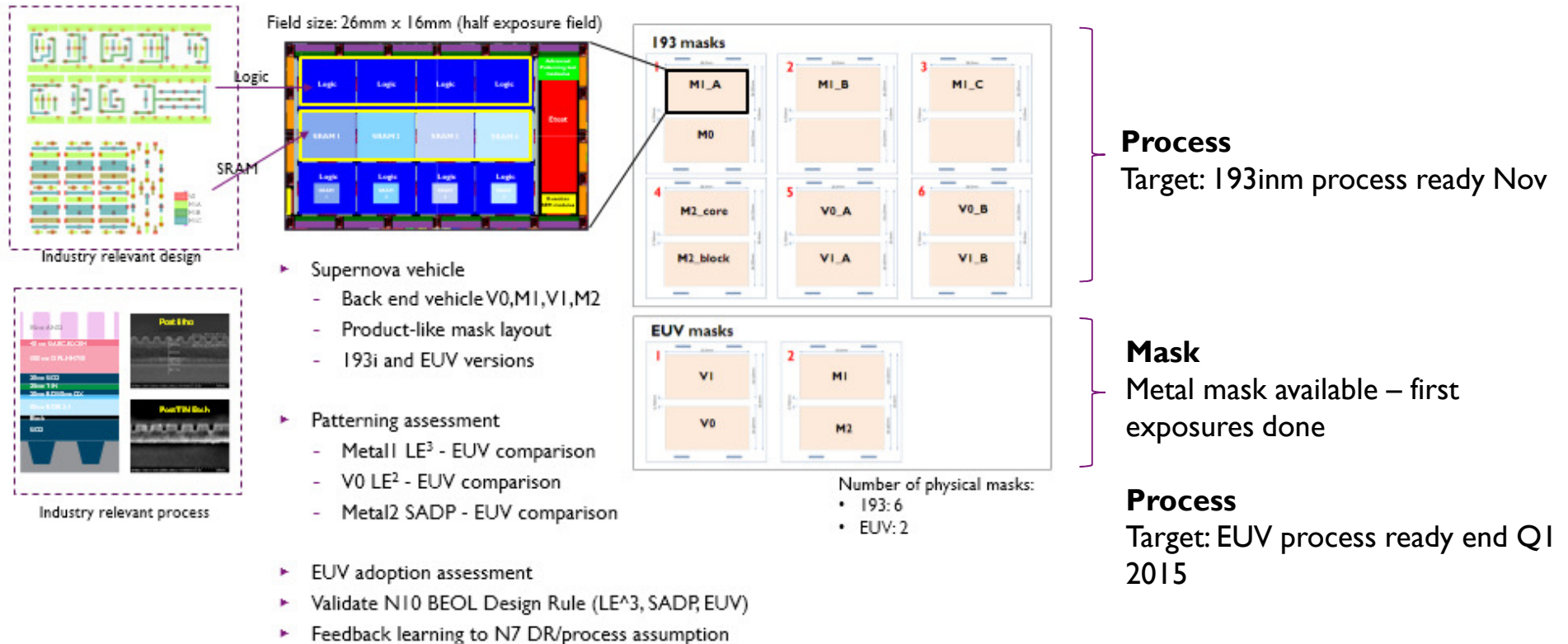
NXE:3300 CLUSTER

STATUS AND OUTLOOK

Date	Milestone	Status
March 2013	TEL Lithius Pro-Z mechanical install	Done
Q3 2013	Lithius Pro-Z SAT and EUV resist installation	Done
Wk37-39	NXE:3300 Beam Transport System installation at imec	Done
Wk40	NXE:3300 Drive laser installation at imec	Done
	First light in NXE:3300 source in VHV	Done
Wk 41.5	Start prepack of scanner in VHV	Done
Wk43.3 2014	Scanner target shipment date, system assembly in imec cleanroom	Ongoing
Wk05.5 2015	Finish NXE:3300 SAT	

Scanner is being installed at imec
SAT completed target wk05.5, 2015

N10, N7 SCALING VEHICLE FOR NXE:3300 EUV LEARNING

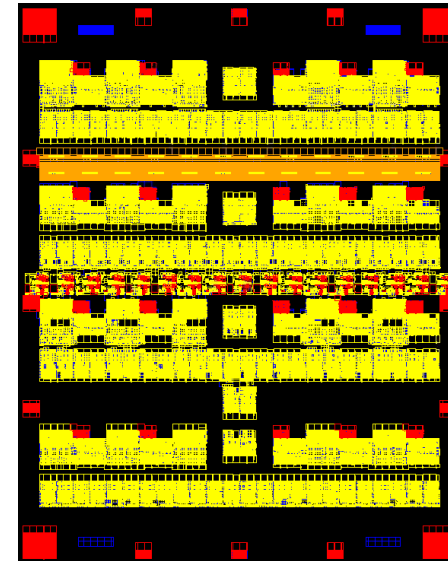


Backend shortloop vehicle process work for N10, N7 learning and EUV – 193i comparison is starting

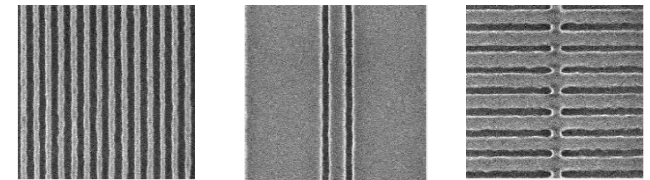
OPC MODEL CALIBRATION ON NXE:3300

NI0, N7 METAL AND VIA LAYERS

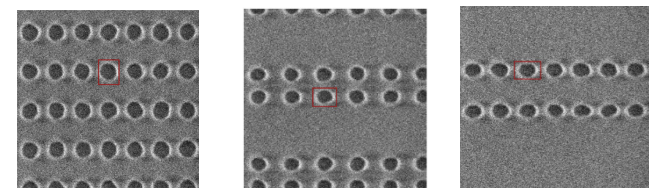
- ▶ Dedicated EUV model calibration mask was generated
 - Through pitch patterns, 2D patterns
 - Shadowing: patterns across slit
 - Flare: different densities
 - Features in mask corners, at field edges
- ▶ Mask has dark image border, which reduces (but not eliminates) die-die interaction
- ▶ Mask exposed on NXE:3300 in DEMO at ASML VH V
- ▶ Model calibration data collected on Hitachi CG-5000 using automated recipe setup



Metal



Via

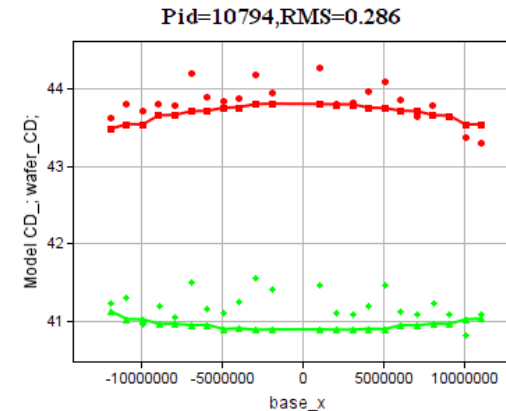


OPC MODEL CALIBRATION ON NXE:3300

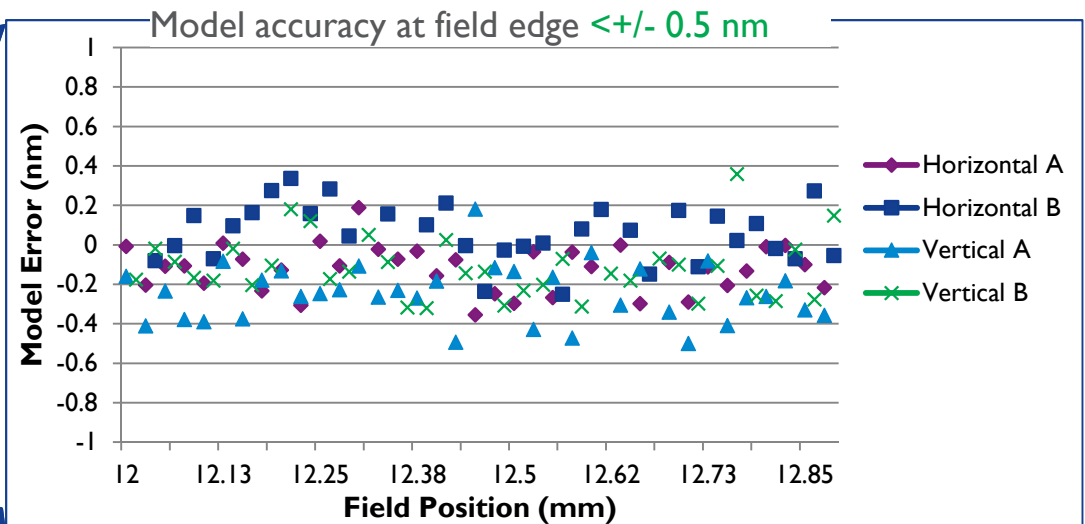
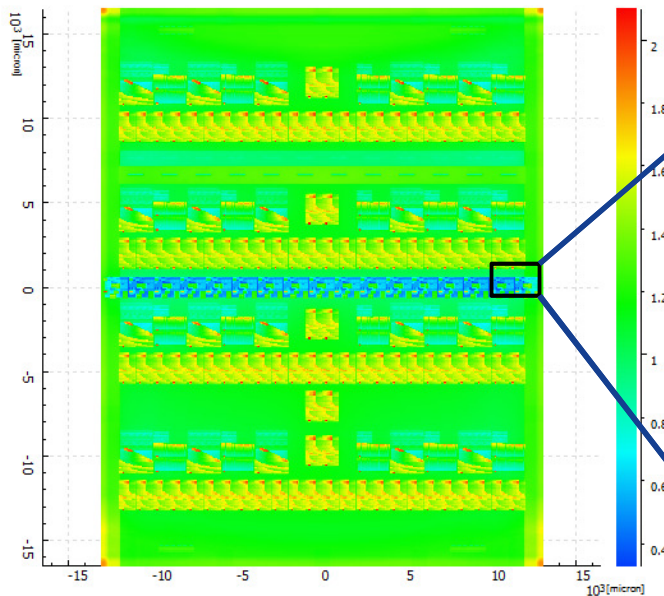
NI0, N7 METAL AND VIA LAYERS

- ▶ ASML-Brion Tachyon NXE model captures EUV specific effects
 - Shadowing: patterns across slit
 - Flare: flare map accurately models CD evolution near field edge due to die-die interaction
 - Final rms total model errors of 0.6-1.0nm

Matching of experimental and modeled CD slit signature



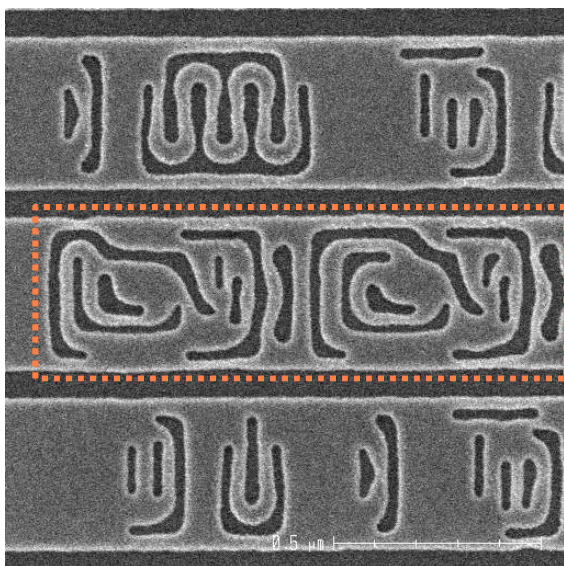
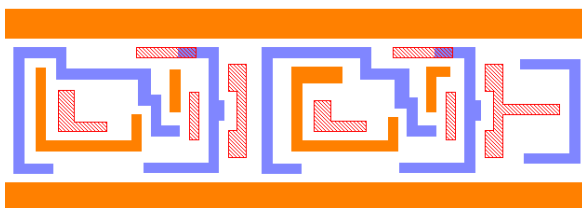
Flare map, including die-die interaction



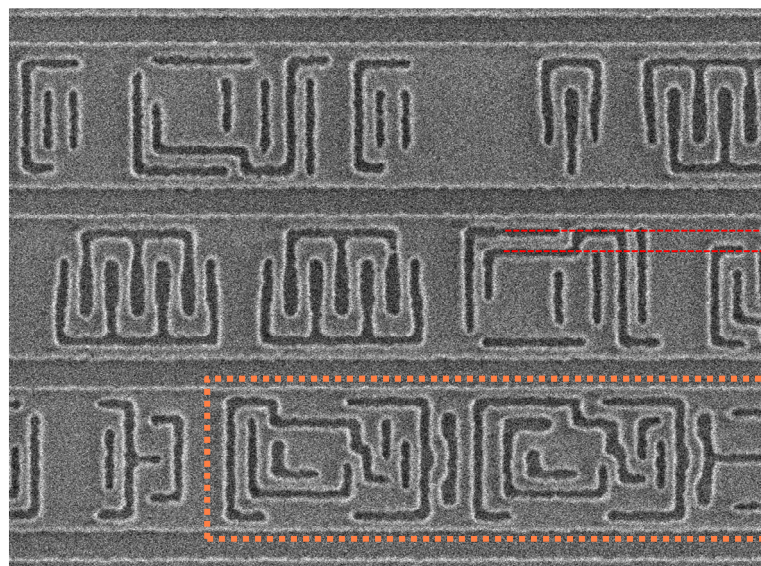
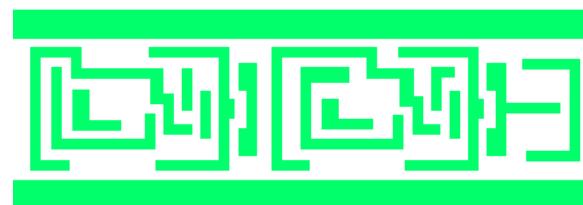
I93I TO EUV COMPARISON FOR NI0/N7 METAL I LAYER

- First EUV exposure done of corrected Metal mask after OPC – NXE:3300

I93i: LE3



EUV single exposure

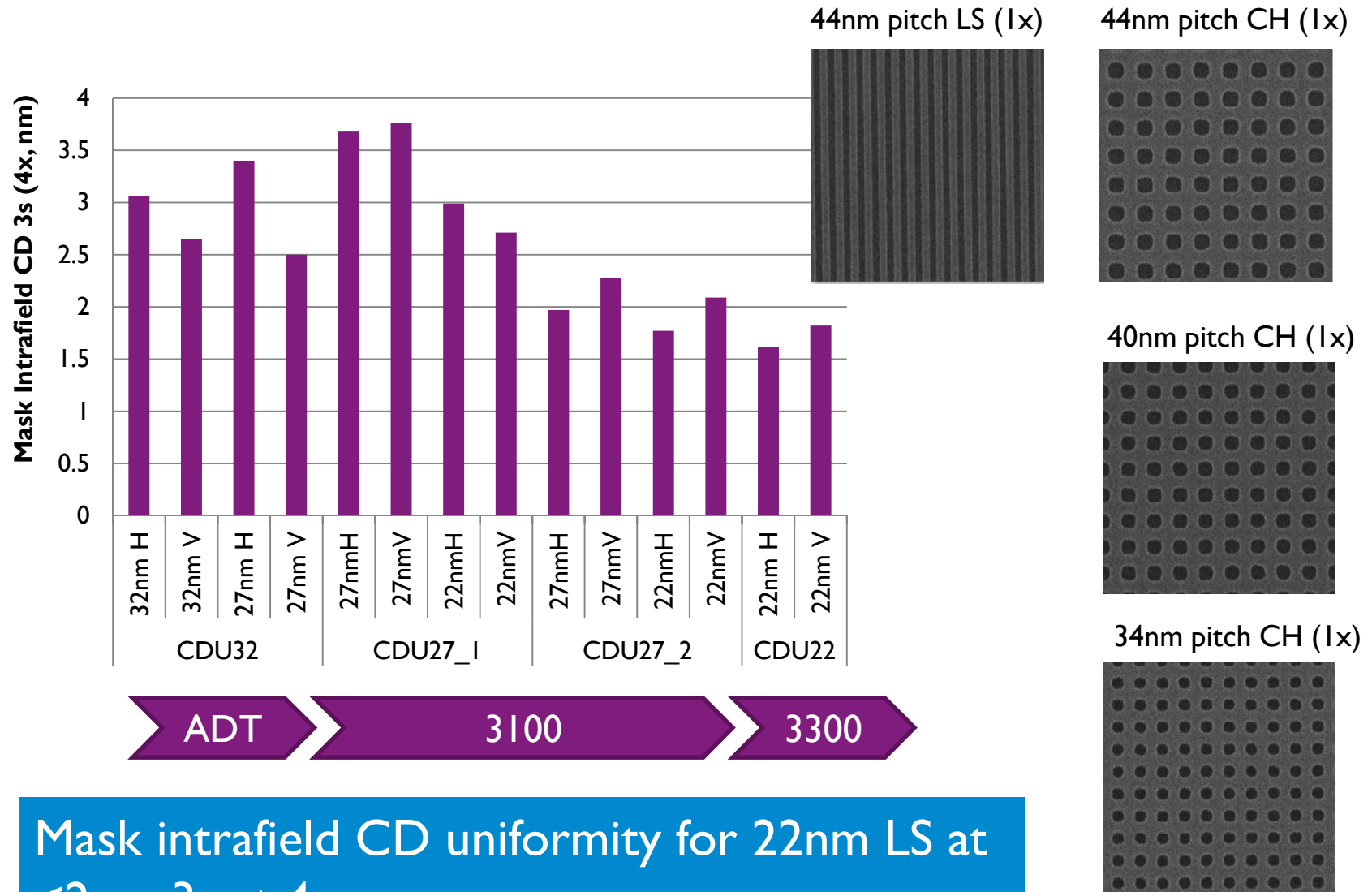


48nm pitch

I93i 3LE route – corner rounding is challenging
EUV single patterning offers clearly better patterning fidelity than I93i 3 LE

NXE:3300 MONITOR MASK

ABSORBER WIDTH UNIFORMITY ON MASK



Mask intrafield CD uniformity for 22nm LS at <2nm 3s at 4x

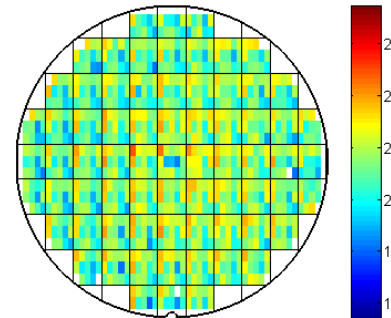
NXE:3300 PROCESS SETUP TEST ON NXE:3100

22NM LS PROCESS CD UNIFORMITY

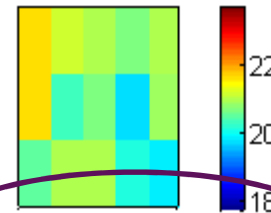
- ▶ NXE:3300 Process setup on TEL Lithius Pro-Z – exposure on NXE:3100
- ▶ 3100 monitor mask vs. 3300 monitor mask with etched ML border
- ▶ Conditions
 - Dipole 60-X illumination
 - Full wafer and full field exposure
 - CD measured in 3 x 5 field positions, including field edges
 - Raw data reported – no corrections applied

Smaller intrafield CD signature is consistent with improved mask quality

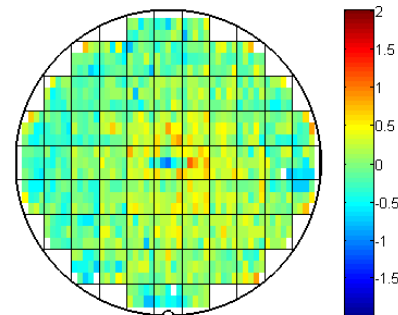
NXE:3100 mask



Total 1.86nm 3s

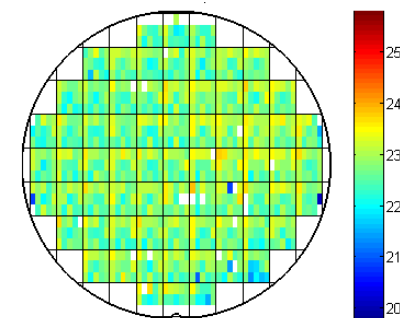


Intrafield 1.70nm 3s

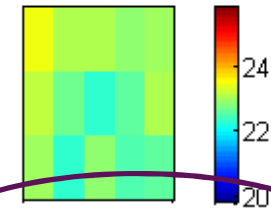


Intrafield subtracted
0.89nm 3s

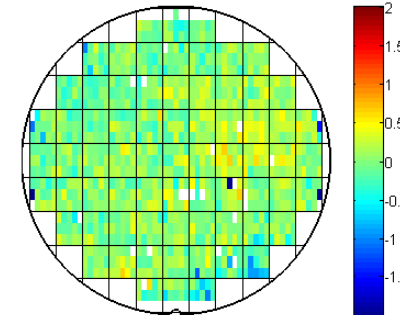
NXE:3300 mask



Total 1.27nm 3s



Intrafield 0.99nm 3s

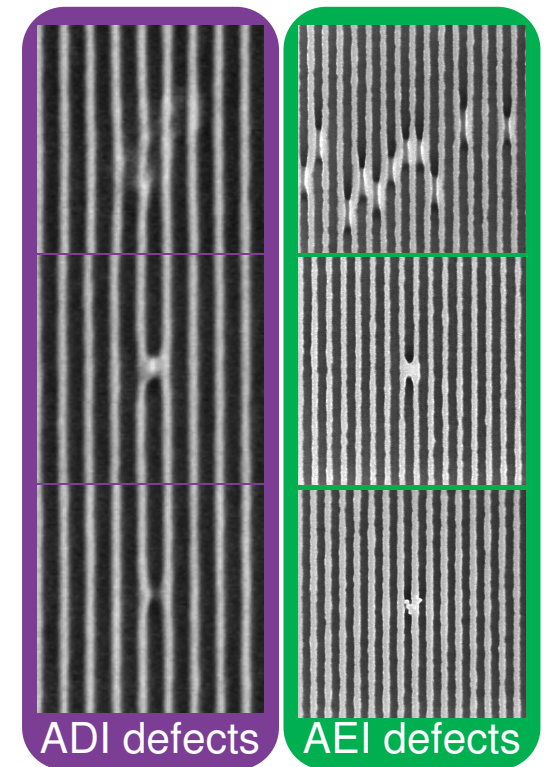
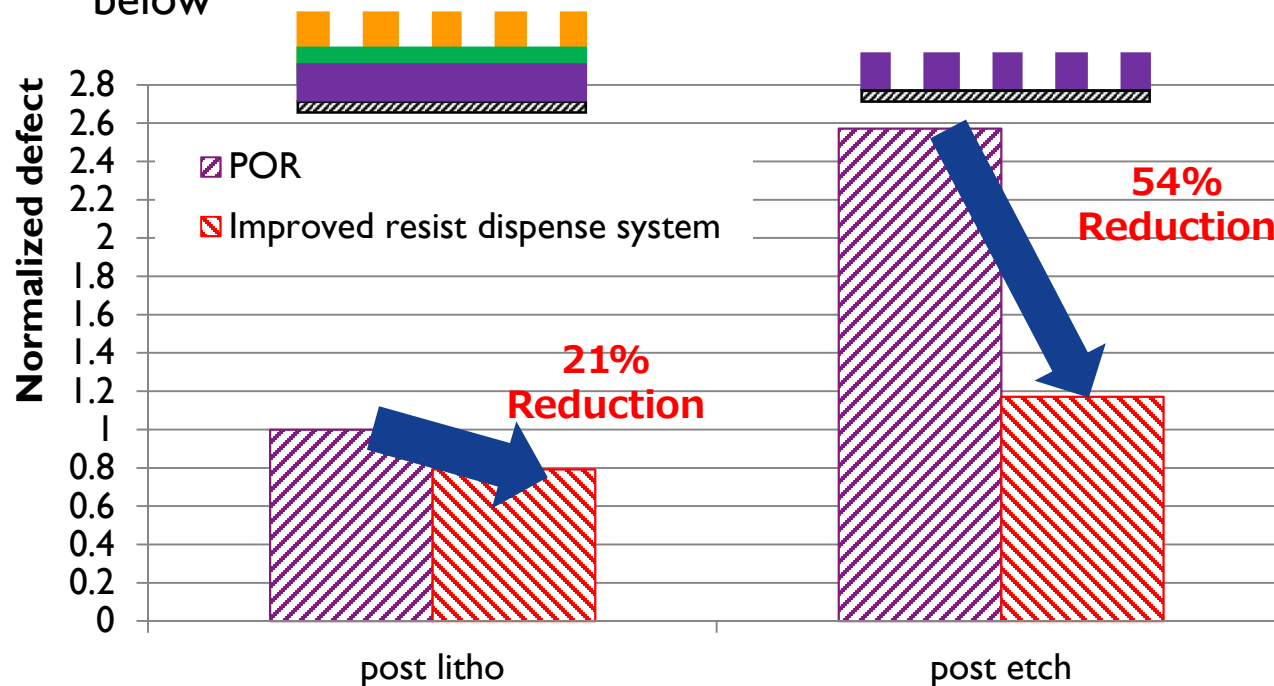


Intrafield subtracted
0.83nm 3s

NXE:3300 PROCESS SETUP TEST ON NXE:3100

PROCESS DEFECTIVITY IMPROVEMENT

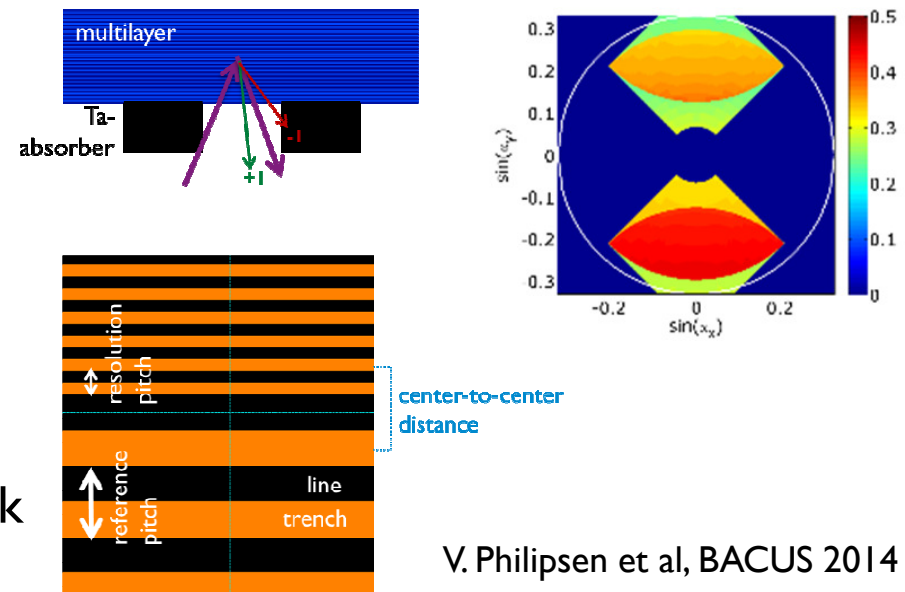
- ▶ NXE:3300 Process setup on TEL Lithius Pro-Z
- ▶ Improved resist dispense system reduces coating particles post etch compared to conventional dispense – defects classified as coating defects after review are below



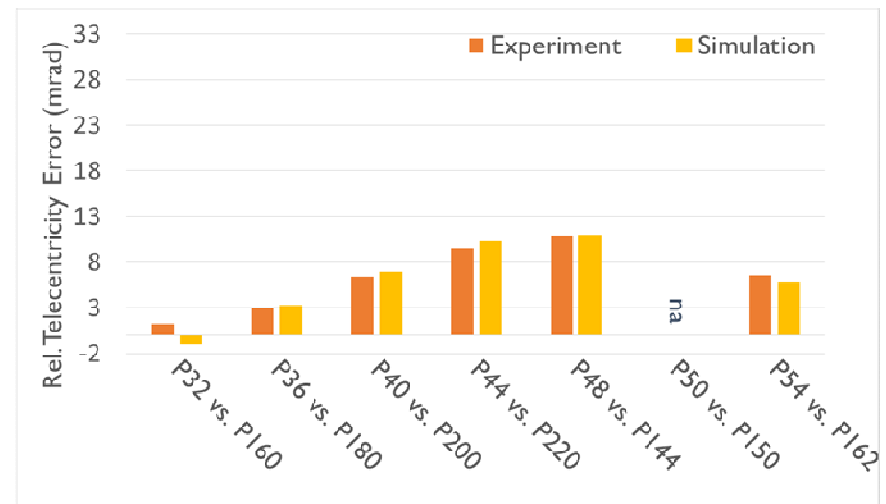
Improved resist dispense system reduces coating particles and post etch defect density compared to conventional dispense

NXE:3300 MASK PERFORMANCE VALIDATION ACROSS SLIT CD VARIATION

- ▶ NXE:3300 exposure
- ▶ Mask 3D effect causes pupil non-telecentricity, leading to pattern-dependent placement error through focus
- ▶ Measured pattern placement error through focus
- ▶ Detailed modeling, including mask stack model can match experiment
 - SLitho-EUV (Synopsys)
- ▶ Effect is small for standard EUV mask stack (1nm placement for 100nm defocus)
- ▶ New mask technologies can further reduce these effects



V. Philipsen et al, BACUS 2014



Session XI: Alternative EUV Mask Technology for Mask 3D Effect Compensation Lieve Van Look

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NXE: 3300

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CONCLUSIONS

NXE:3100	
Throughput	More than 9000 wafers exposed (3 years) Source collector mirror influences power level ~6-9 months collector mirror lifetime
Resists	CAR <u>not</u> reaching targets for LVR\Dose tradeoff CAR enablement needs to confirm good performance Inorganic materials will need time to mature
Masks	Good progress in mask FS particle adders Mask frontside cleaning up to 100x – no CD impact

NXE:3300	
Throughput	Expect 30 wph in Q1 2015
Process	TEL Lithius Pro-Z track ready, resists selected
Mask	First OPC modelcalibration, mask fabrication exercises completed – N10 masks available





Thank you for your attention

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